ABSTRACT

An architecture for creating a vertical JFET. Generally, an integrated circuit structure includes a semiconductor area with a major surface formed along a plane and a first source/drain doped region formed in the surface. A second doped region forming a channel of different conductivity type than the first region is positioned over the first region. A third doped region is formed over the second doped region having an opposite conductivity type with respect to the second doped region, and forming a source/drain region. A gate is formed over the channel to form a vertical JFET.

In an associated method of manufacturing the semiconductor device, a first source/drain region is formed in a semiconductor layer. A field-effect transistor gate region, including a channel and a gate electrode, is formed over the first source/drain region. A second source/drain region is then formed over the channel having the appropriate conductivity type.